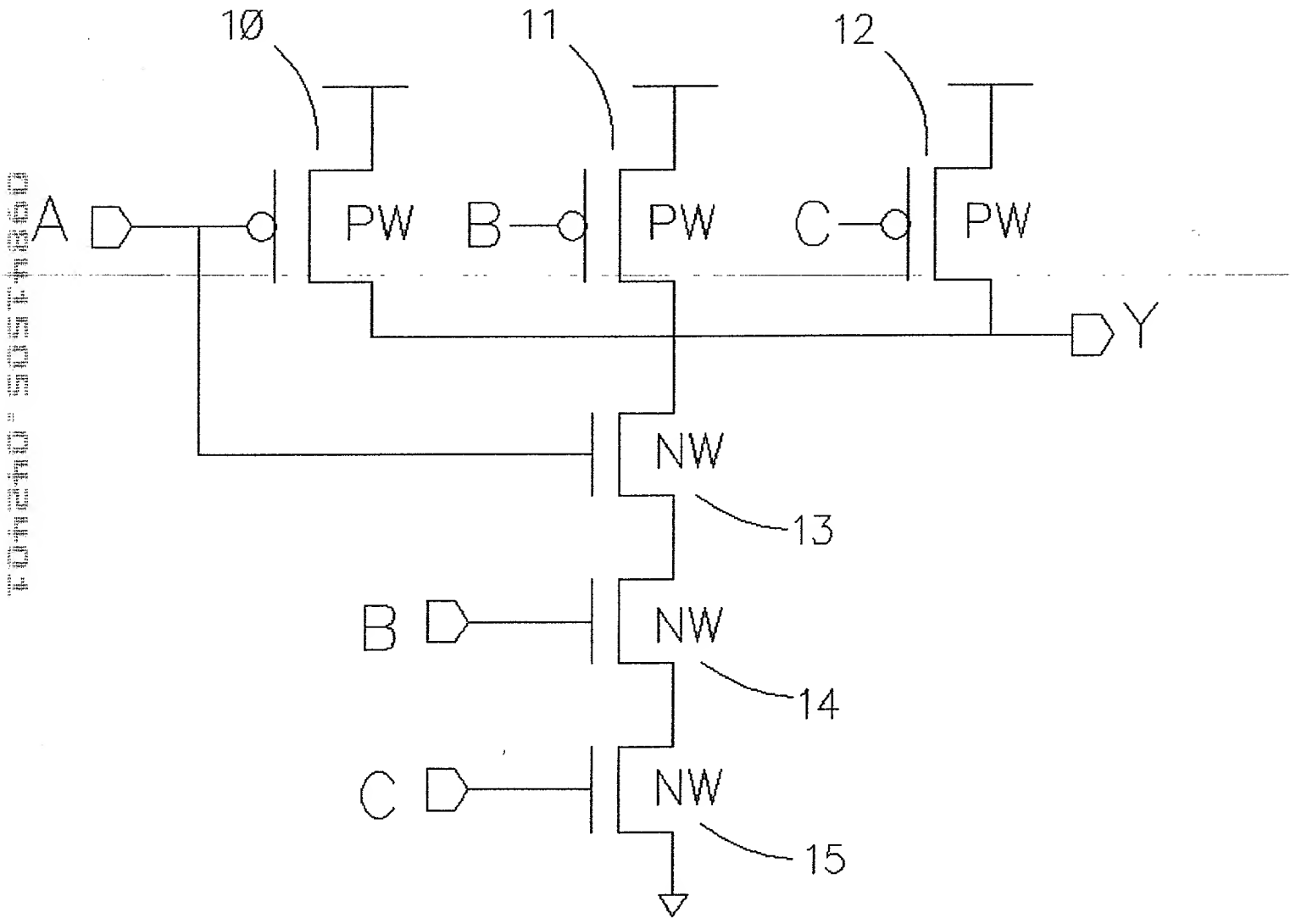


Fig 1. Non-tapered 3-input CMOS NAND gate

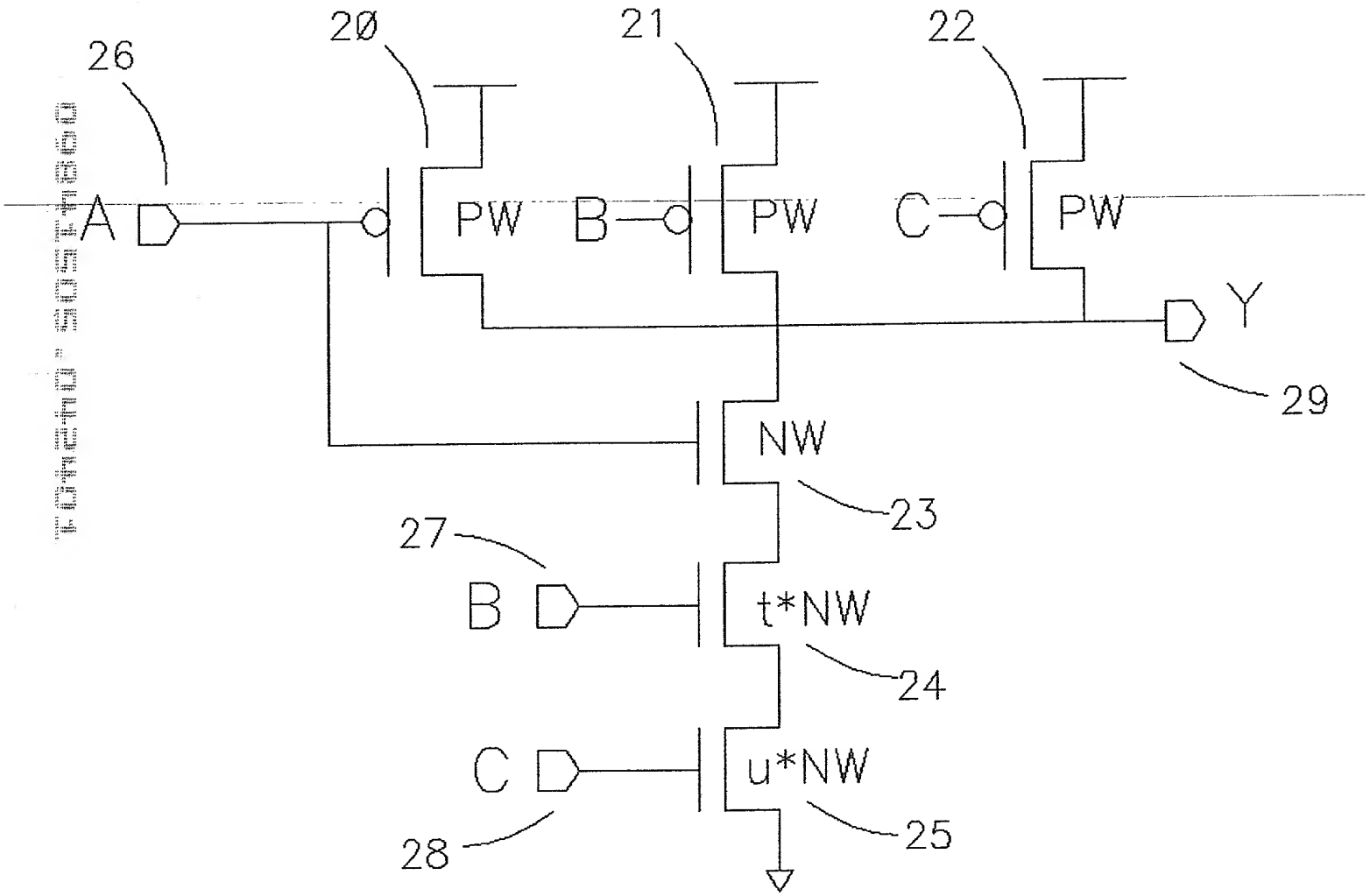


Fig 2. Tapered 3-input CMOS NAND gate

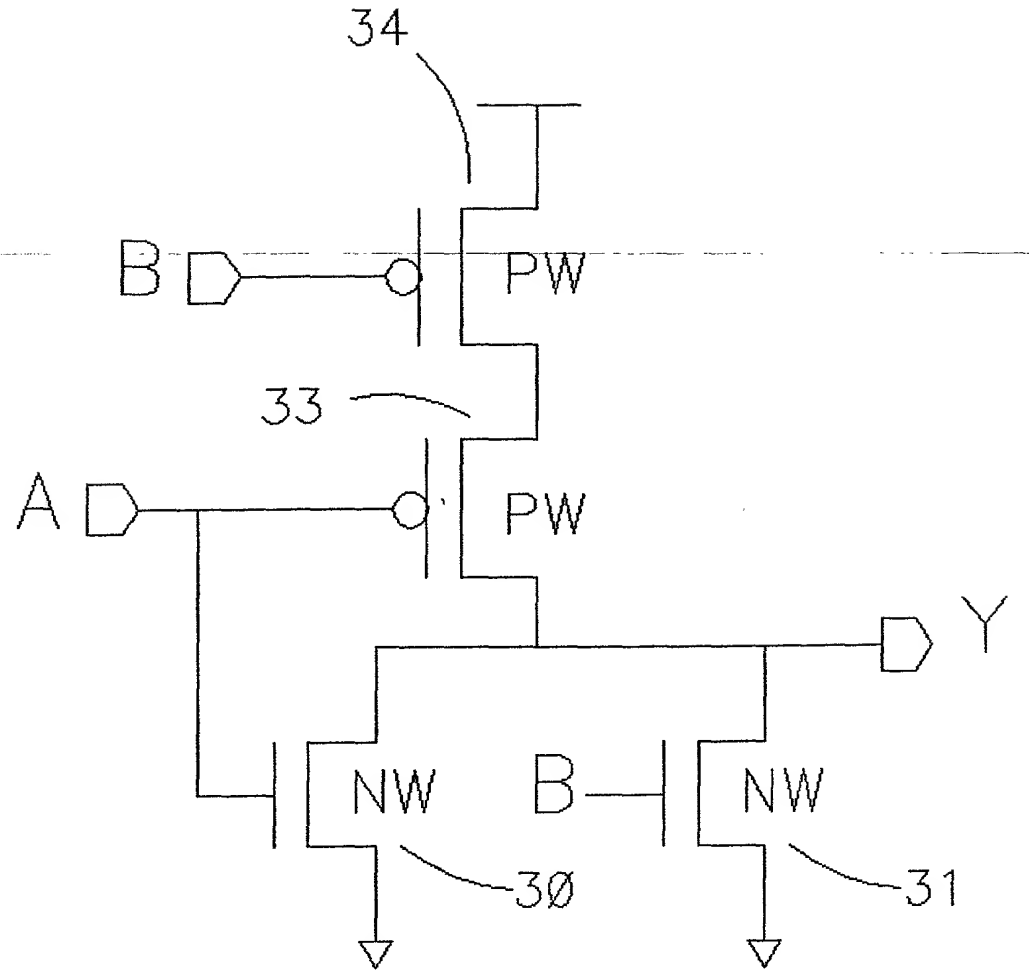


Fig 3. Non-tapered 2-input CMOS NOR gate

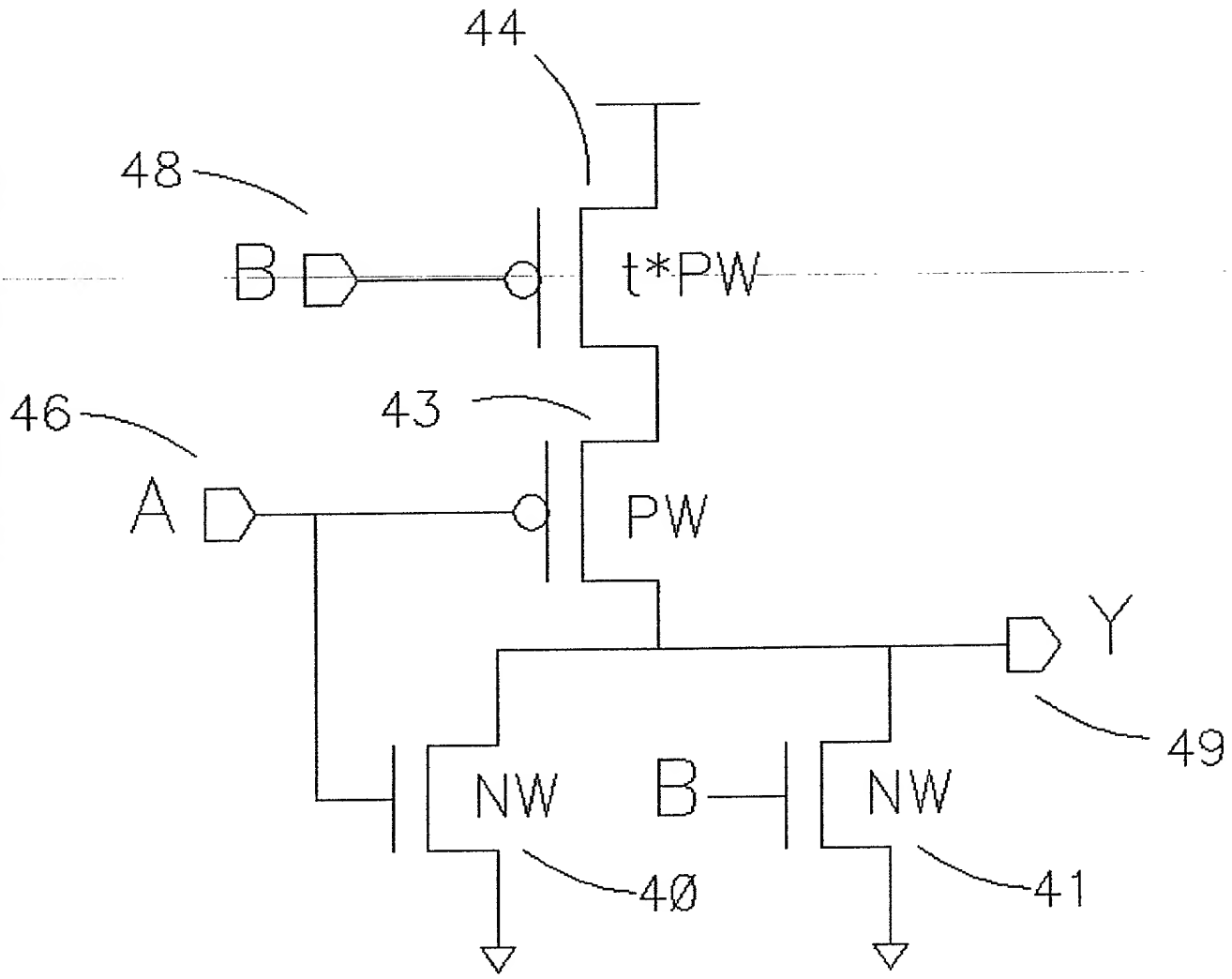
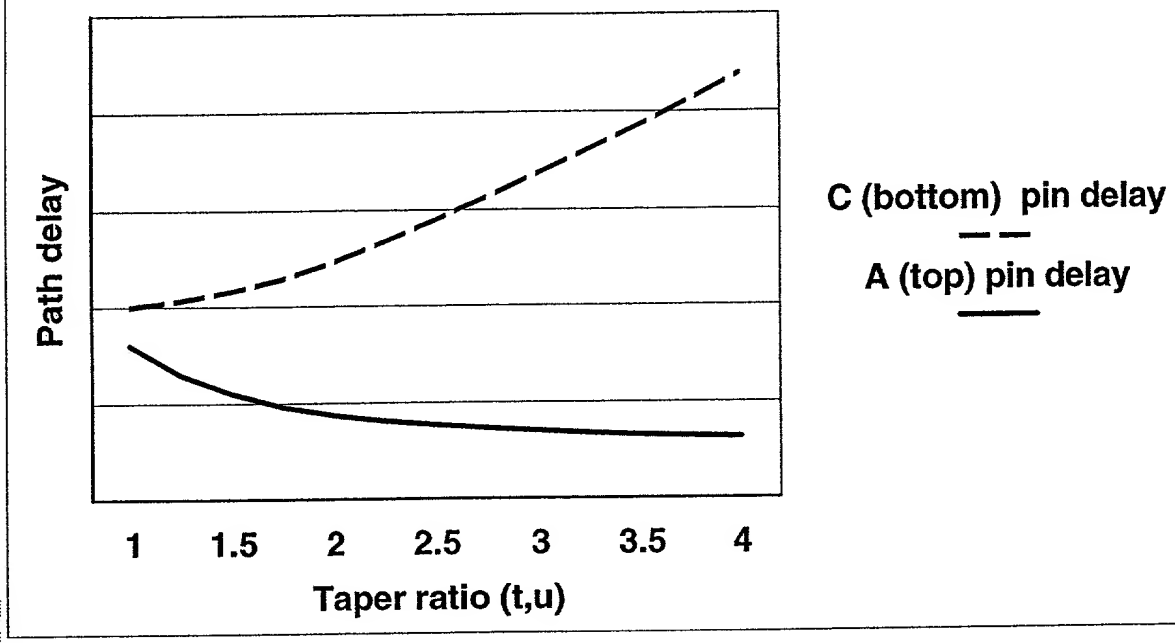


Fig 4. Tapered 2-input CMOS NOR gate

Fig. 5. 3-input NAND Path Delay vs. Taper Ratio



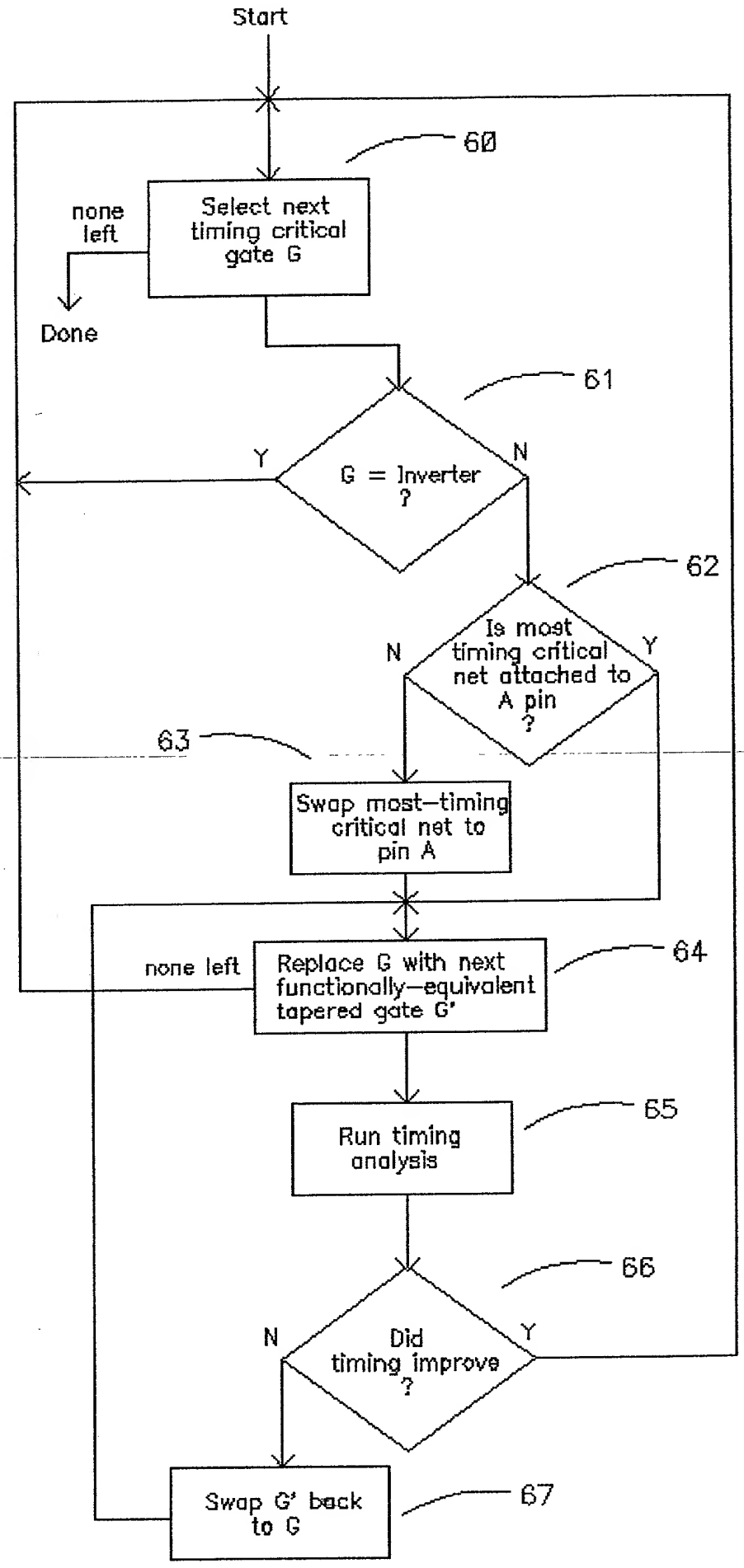


Fig 6. Synthesis tapered algorithm